Biyani's Group of Girls' Colleges

Model Paper – I

Examination-2016

BCA III

Advanced Computer Architecture

Time: 3 Hrs. MM:50

I) The Question paper contains 40 multiple choice questions with four choices and student will have to pick the correct one (each carrying ½ mark).

1. .....is a technique of decomposing a sequential process into sub operations.
   (a) Pipelining (b) Parallel Processing
   (c) Vector Processing (d) None of the above ( )

2. Personal computer were appeared in:
   (a) Ist generation (b) 2nd generation
   (c) 4th generation (d) 5th generation

3. A.....contains the address of the next instructions to be executed.
   (a) Data Register (b) Accumulator
   (c) Instruction Register (d) Program Counter

4. A.....is an interconnected set of processing elements which cooperate by communicating with one another to solve large problem
   (a) Parallel Computer (b) Personal Computer
   (c) Laptop Computer (d) None of the above

5. MIPS stands for:
   (a) Memory Instruction Per Second (b) Major Instruction Per Second
   (c) Main Information Per Second (d) Million Instruction Per Second

6. A.....can be be visualized as a collection of processing segments through which binary information flows:
   (a) Memory (b) I/O devices
   (c) Processor (d) Pipeline

7. A typical system bus consists of approximately.....signals lines
   (a) 100 (b) 2
   (c) 3 (d) None of the above

8. M.J. Flynn's parallel processing classification is based on:

(a) Multiple Instructions (b) Multiple data
(c) Both (a) and (b) (d) None of the above

9. The channel width of a .....network increases as we ascend from leaves to the root.
(a) Binary fat tree (b) Star
(c) Ring (d) Binary tree

10. TLB is used in:
(a) Paging (b) Segmentation
(c) Both (a) and (b) (d) None of the above

11. VLIW stands for:
(a) Vector Large Instruction Word (b) Very Long Instruction Word
(c) Very Large Integrated Word (d) Very Low Integrated Word

12. The major disadvantage of pipeline is:
(a) High cost individual dedicated
(b) Initial setup time
(c) If branch instruction is encountered the pipe has to be flushed
(d) All of the above

13. Which of the example of blocking network?
(a) Baseline (b) Delta
(c) Omega (d) All of the above

14. Data routing functions include:
(a) Shifting and rotation (b) Permutation
(c) Shuffle and Exchange (d) All of the above

15. Throughput is measure of:
(a) Number of instruction set executed per unit of time
(b) Time for the completion of the task
(c) Work done by the CPU
(d) Memory Speed

16. In a UMA multiprocessor model all processor have.....access time to all memory words:
(a) Asynchronous (b) Equal
(c) Different (d) None of the above

17. Cache memory is:
(a) Temporary and costly (b) Primary
(c) High speed memory (d) All of the above

18. What does RISC stand for?
(a) Register Instruction Set Counter (b) Reduced Instruction Set Computer
(c) Reduced Instruction Set Counter (d) Register Instruction Set Computer

19. A computer system consists of a CPU, a memory and one or more specialized I/O processor called:
(a) Bandwidth (b) Data Channels
(c) Interrupt (d) None of the above

20. Which of not an address mapping scheme:
    (a) Associate Mapping
    (b) Direct Mapping
    (c) Direct Associate Mapping
    (d) Set Associate Mapping

21. Example of zero address instruction is:
    (a) ADD B
    (b) ADD
    (c) ADD R1, B
    (d) ADD R1, A, B

22. The speed of microcomputer measure in:
    (a) MIPS
    (b) Picoseconds
    (c) Megahertz
    (d) Milihertz

23. Memory interleaving is:
    (a) Modular memory
    (b) Virtual memory
    (c) Shared memory
    (d) Cache memory

24. Virtual memory is:
    (a) A part of main memory
    (b) Shared memory
    (c) Part of cache memory
    (d) A mechanism to process fast

25. Which mode transits data in both directions, but not at the same time:
    (a) Simplex mode
    (b) Half duplex mode
    (c) Full duplex
    (d) None

26. Two or more CPU's present in a computer system which share some or all of the memory called:
    (a) Paralleled
    (b) Multiprogramming
    (c) Multi tasking
    (d) Random File processing

27. Which is not valid architecture of a vector super computer?
    (a) Register to register
    (b) Memory to memory
    (c) Both a and b are invalid
    (d) None of the above

28. The total number of messages the network can handle is:
    (a) Network efficiency
    (b) Network throughput
    (c) Network output
    (d) All of the above

29. Instruction issue latency is:
    (a) Clock period of instruction pipeline
    (b) Time required between issuing of two adjacent instruction
    (c) No. of instructions issued per cycle
    (d) No. of cycles required by an instruction

30. For pattern recognition, which processor is used
    (a) Vector
    (b) Symbolic
    (b) VLIW
    (d) Superscalar

31. The relationship between access frequencies among different level of memory is:
    (a) f1>>f2>>f3…….>>fn
    (b) f1<<f2<<f3…….<<fn
    (c) f1=f2=f3…..=fn
    (d) None of the above

32. Which network suffers from bottleneck problem:
    (a) Mesh (b) Binary tree
    (c) Systolic Array (d) Hypercube

33. Which computation corresponds to Lazy evaluation:
    (a) Control Flow (b) Data Flow
    (c) Demand Driven (d) All of the above

34. In which model, each demander gets a separate copy of the expression for its evaluation:
    (a) String-Reduction Model (b)Graph Reduction Model
    (c) Both (a) and (b) (d) None of the above

35. Multiprocessor is one with:
    (a) One CPU executing several processor (b) Several CPU
    (c) One CPU and several channels (d) None of the above

36. .....Networking is controlled by a global clock.
    (a) Asynchronous (b) Synchronous
    (c) Both (a) and (b) (d) None of the above

37. To find out cache performance we can use:
    (a) Program trace driven simulation (b) Hit ration
    (c) Greedy cycles (d) Cycle Count

38. An/a .....is a request from I/O or other devices to a processor for services or attention:
    (a) Transaction (b) Arbitration
    (c) Interrupt (d) None of the above

39. Router is a :
    (a) Data Transfer protocol (b) Networking device
    (c) Modem (d) None of the above

40. LRU stands for:
    (a) Last recently used (b) Least Recently used
    (c) Last Rarely Used (d) Least Rarely Used

II) Attempt any four questions out of the six. All questions carry 7½ marks each.

Q1. What do you understand by shared memory multiprocessor and distributed memory multi computers? Explain different models of shared memory multiprocessor.

Q2. Differentiate between static and dynamic networks. Explain any five types of static connection network.

Q3. What do you understand with virtual memory? Describe the page replacement techniques in virtual memory.

Q4. Explain instruction set architecture in RISC and CISC processor.

Q5. Explain the following terms associated with program partitioning and scheduling:
    a) Grain sizes and latency
    b) Grain packing and scheduling

Q6. What do you mean by vector processing? Explain different types of vector instructions with example.